

FIG. 1
 (PRIOR ART)

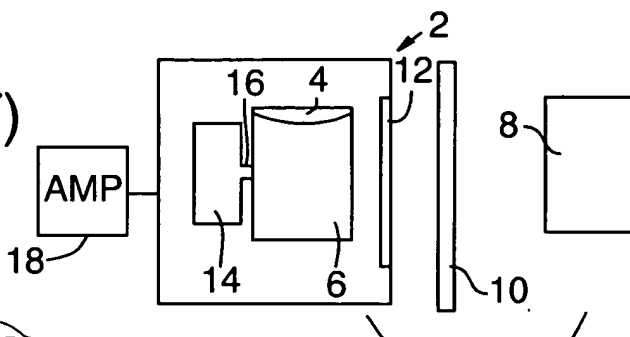


FIG. 2
 (PRIOR ART)

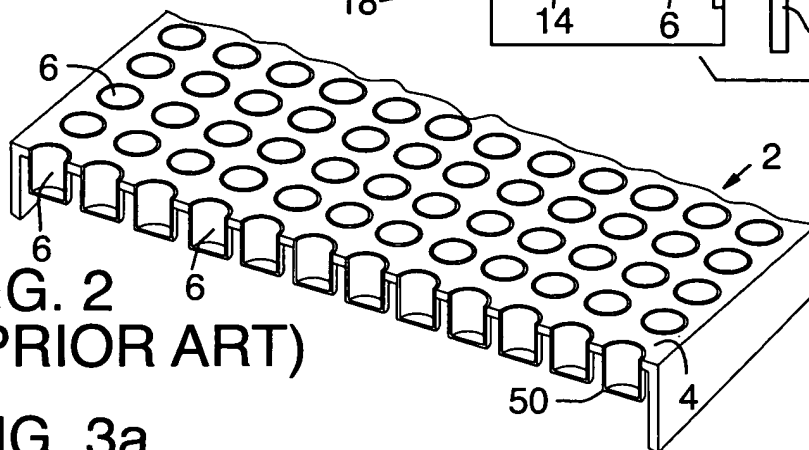


FIG. 3a

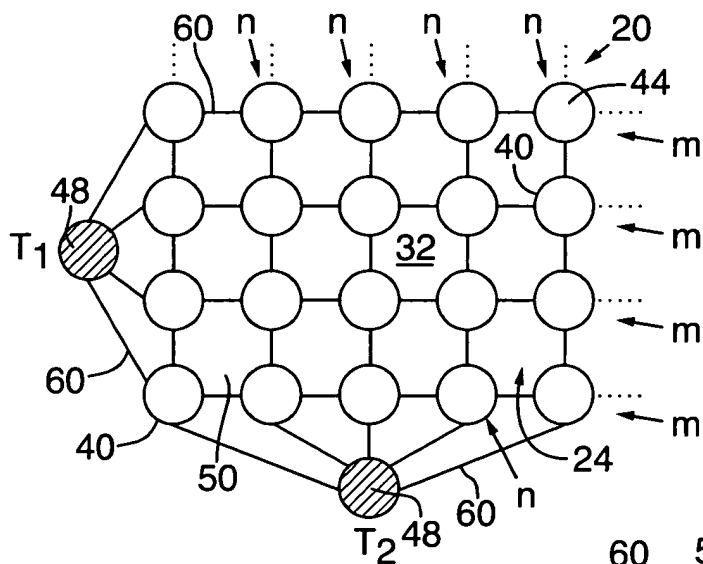


FIG. 3b

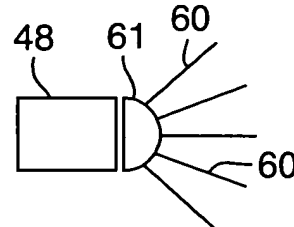


FIG. 4

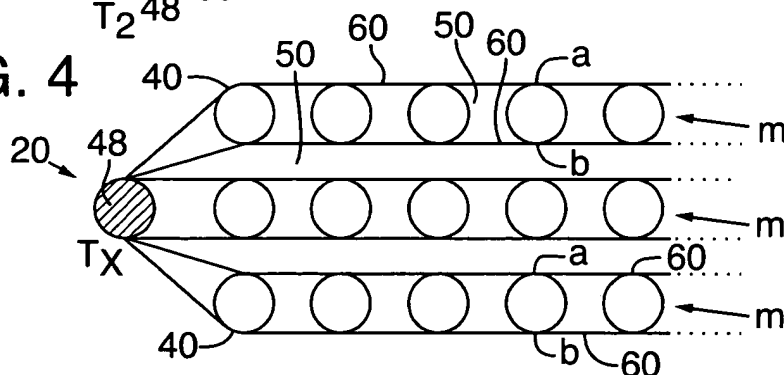


FIG. 5

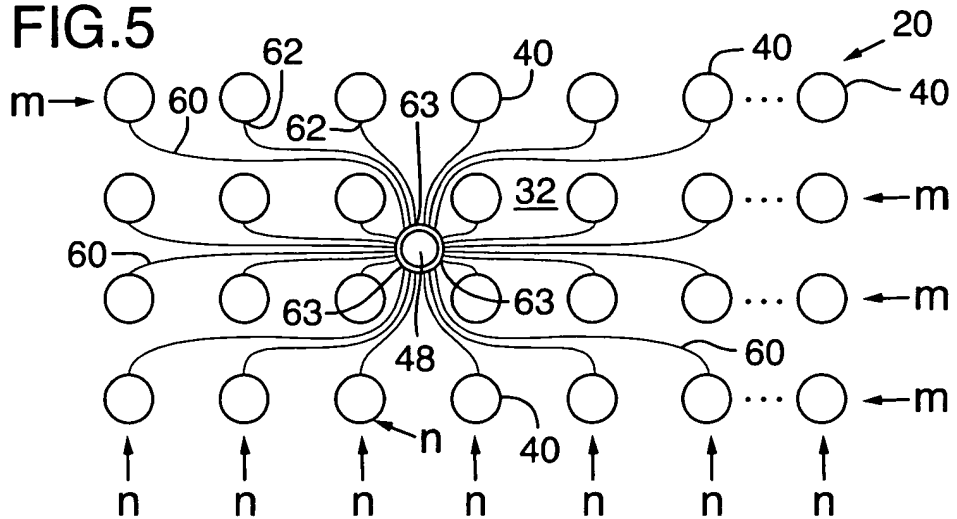


FIG. 6

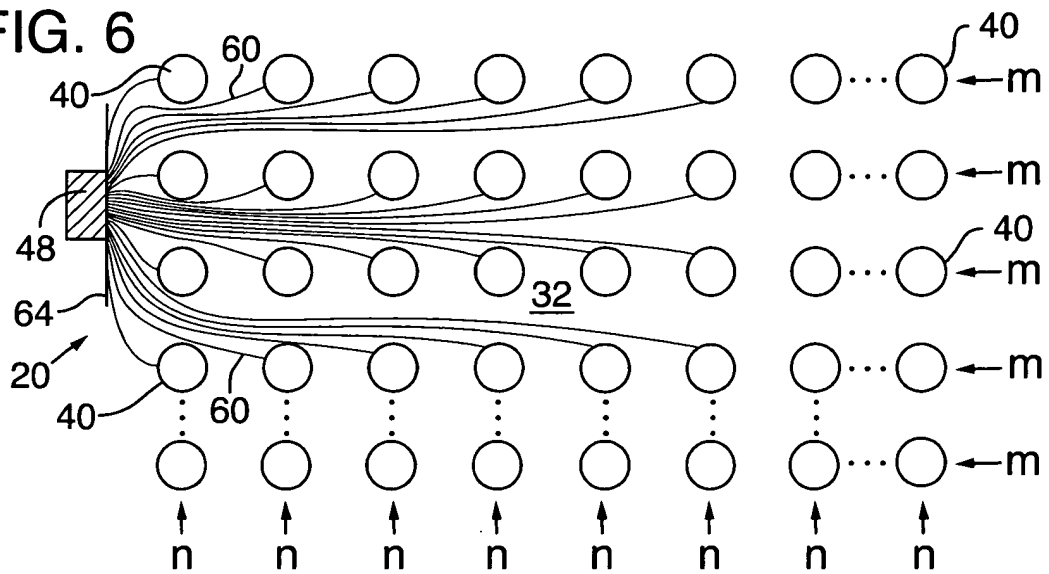


FIG. 7

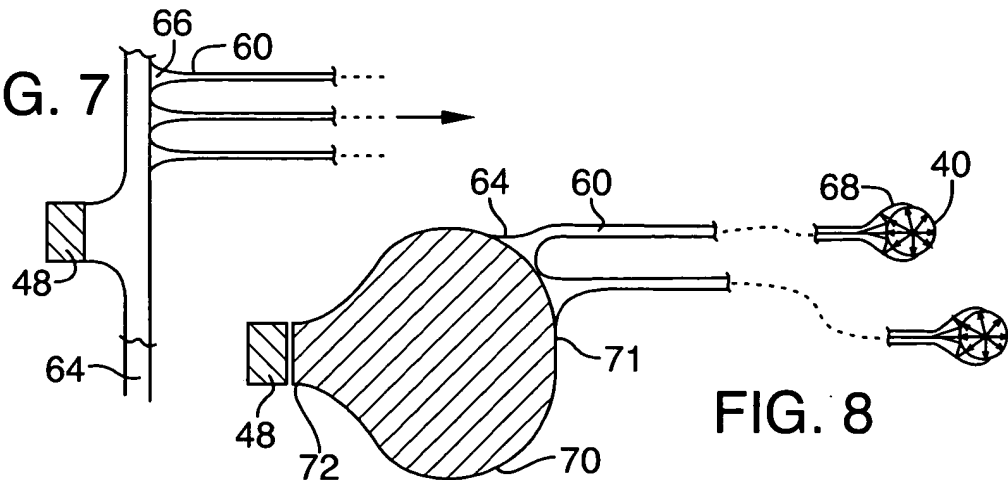


FIG. 8

FIG. 9

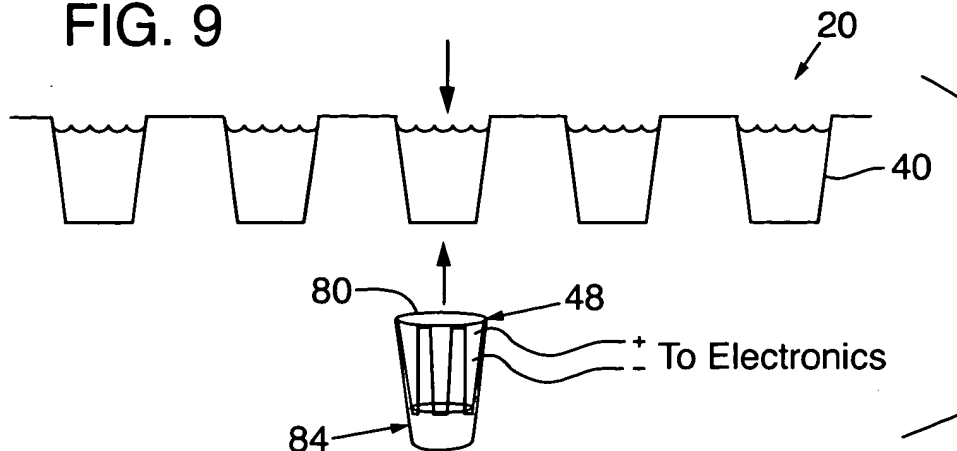


FIG. 10

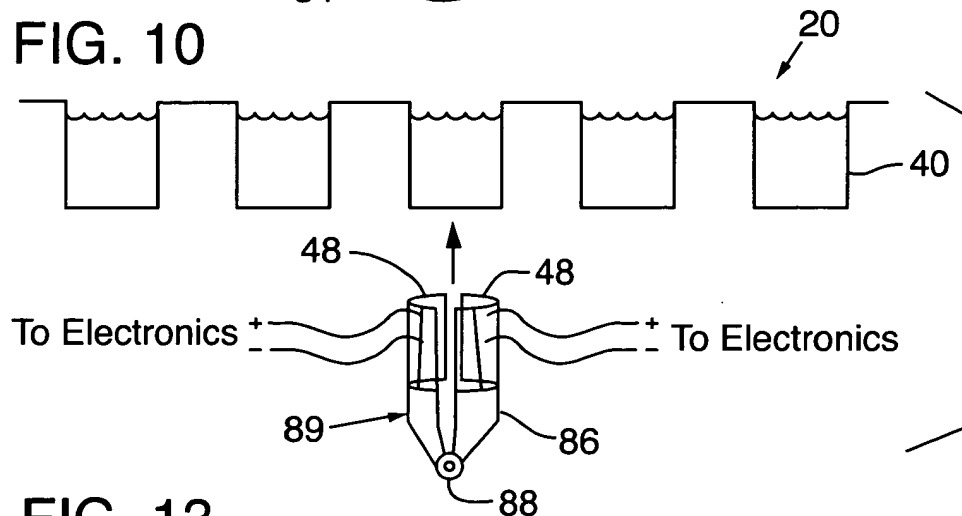
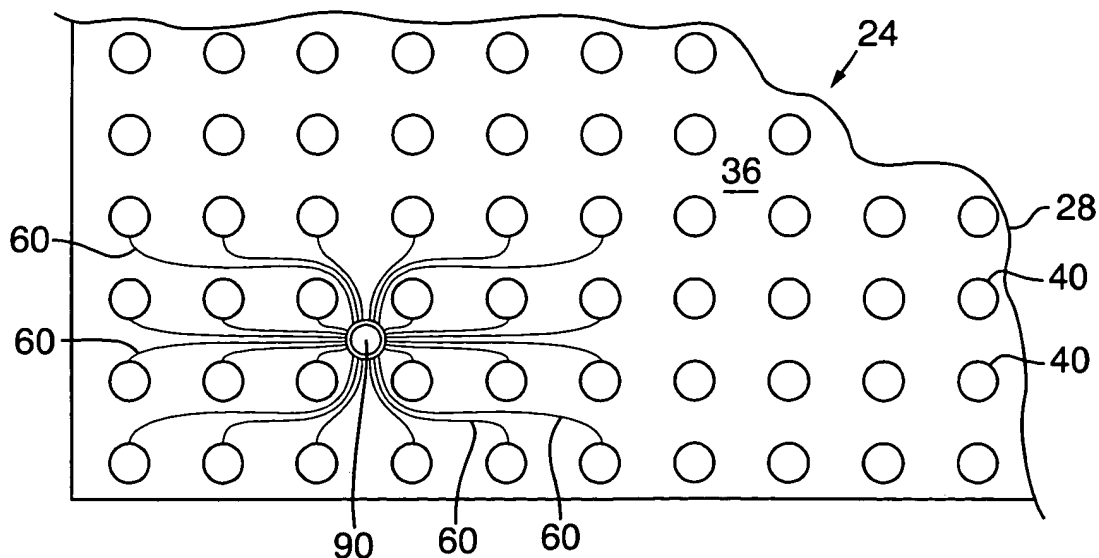
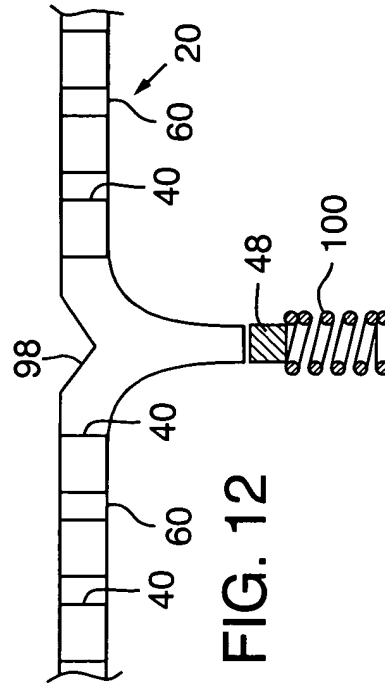
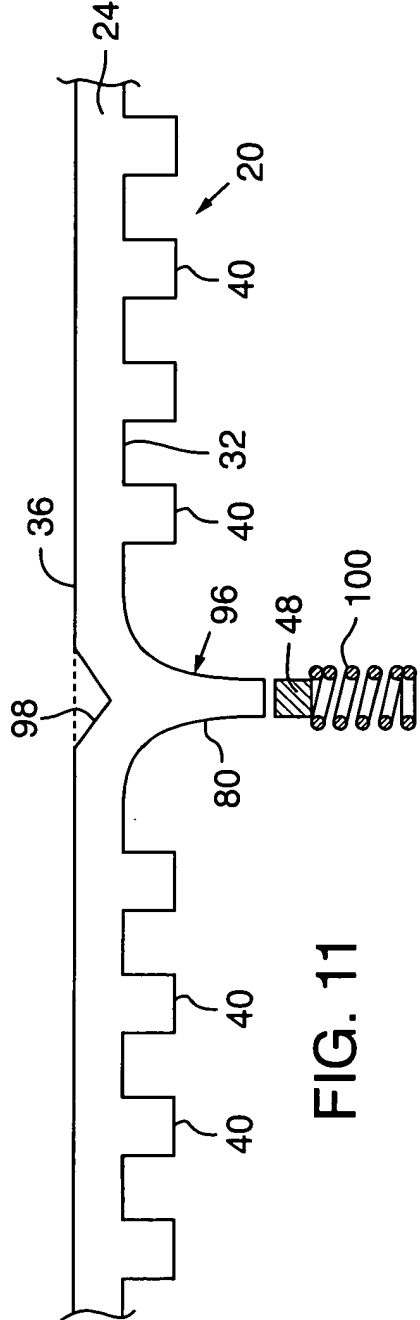


FIG. 13



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ARRAY VESSEL AND ...
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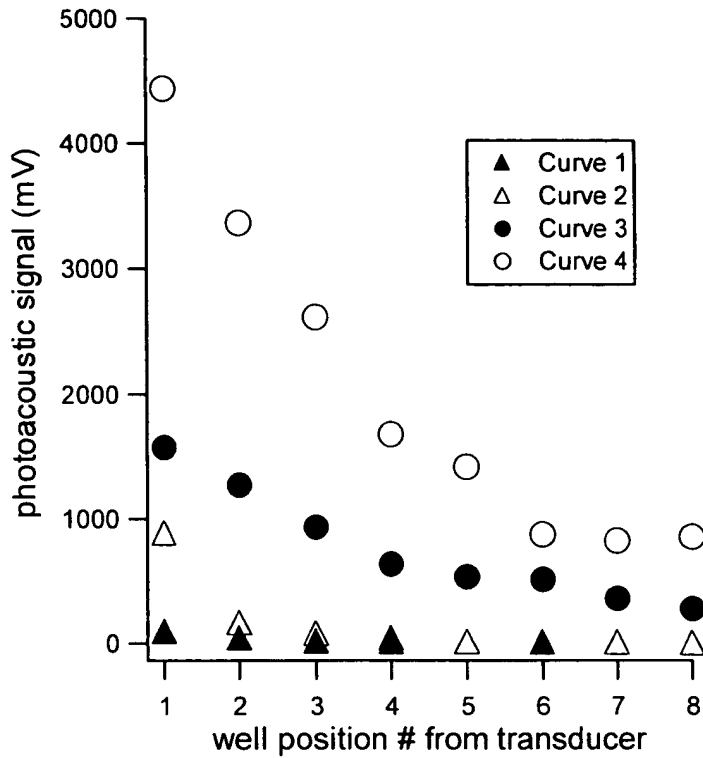


FIG. 14

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FIG. 15a

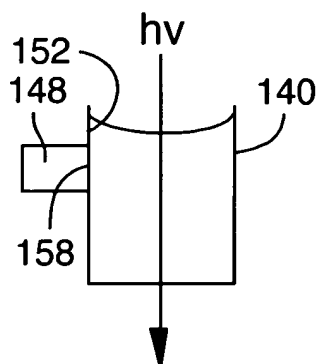


FIG. 15b

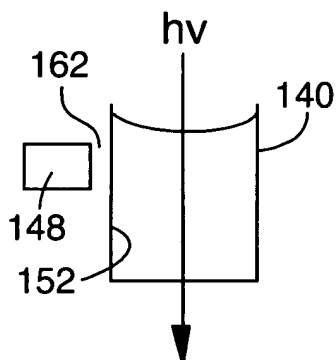
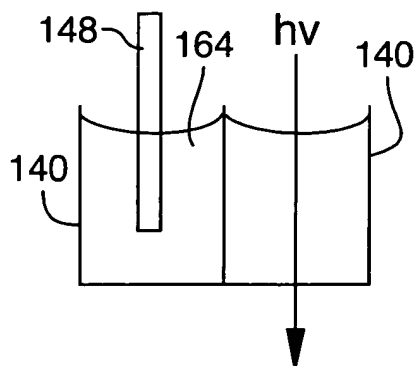


FIG. 15c



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Figure 1 is a cross-sectional view of a semiconductor device. The device includes a substrate 142, a layer 148, a patterned layer 136, and a top layer 120. The top layer 120 has openings 140. A side layer 128 is located on the left side, and a contact layer 138 is located on the right side. The device is divided into two regions, A and B, by a dashed line.

